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Patrick J. O'Shea
O'shea, Getz & Kosakowski, P.C.
1500 Main Street, Suite 912
Springfield,, MA 01115

EXAMINER	
MONDT, JOHANNES P	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/852,123
Filing Date: May 08, 2001
Appellant(s): CZECH ET AL.

Patrick O'Shea (Reg. No.: 35,205) (O'Shea, Getz and Kosakowski, P.C., 1500 Main Street, Suite 912, Springfield, MA 01115
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/19/06 appealing from the Office action mailed 4/20/04.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct with the proviso that "appealed" evidently means "filed a Notice of Appeal", an actual appeal brief was not filed until 12/07/05.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Translation of Wada et al as cited by the US PTO Translation Section.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claim 1*** is rejected under 35 U.S.C. 102(b) as being anticipated by Avery (5,043,782).

With reference to Fig. 7: Avery teaches (cf. "Field of Invention", column 1, lines 6-9) an electrostatic discharge (ESD) protective structure that protects an integrated circuit (cf. "Summary of Invention", first line) connected between a first voltage bus 20 (cf. column 4, line 27) with a first supply voltage (inherent) and a second voltage bus or reference line 22 (cf. column 4, lines 27-28), said electrostatic discharge protective structure comprising:

a plurality of laterally designed bipolar transistors QL (cf. column 6, lines 37-42) each having a first load line connected to the first voltage bus 20 and a second line connected to the second voltage bus 22, wherein said first load lines are electrically parallel and said second load lines are electrically parallel to one another (cf. Fig. 7), each of said (laterally designed bipolar) transistors including a control connection to one of the voltage buses, namely the second voltage bus 22 (cf. Fig. 7).

Avery also teaches a resistor (RS) co-integrated into a semiconductor body preceding the control connection for *all* of the aforementioned laterally designed bipolar transistors QL and QS because said resistor RS is co-integrated into the semiconductor by being constituted as the p-doped substrate (col. 4, l. 22-25 and col. 6, l. 44-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 2-5*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery as applied to claim 1 above, in view of Smith (6,075,271).

On claim 2: Avery also teaches the electrostatic discharge protective structure of claim 1 wherein the semiconductor body has embedded therein at least one emitter zone and at least one collector zone (42 and 44 in Fig. 4, respectively) of first conductivity type, and at least one base zone of second conductivity type (58 in Fig. 4).

Avery does not necessarily teach a well-shaped region inserted into said semiconductor body between said zones of the first conductivity types and said base zone or zones so as to extend the path length charge carriers have to travel to the base zone.

However, the use of a deeper doped region or well to significantly increase the path length that avalanche generated charge carriers have to travel as a means to increase the collector-to-emitter voltage in bipolar transistor dynamics is a method well known in the art, as witnessed by Smith, who, in a patent on a semiconductor device with means against the adverse effects of ESD (electrostatic discharge) (see title,

abstract and "Field of the Invention"), hence analogous art, teaches a deeper doped region or well-shaped region 80 (cf. abstract, lines 12-17, and Fig. 7) acting as a barrier for the avalanche-generated charge carriers involved in bipolar snap-back by blocking said charge carriers laterally, increasing the path length to be traversed by them, whereby a higher percentage of them reach the substrate 65 instead and are thus shunted to ground. Because of the specifically stipulated *motivation* as given above and the field of application, namely: technology to increase the bipolar snapback problem, it would have been obvious to one of ordinary skills in the art to modify the invention as essentially taught by Avery so as to include the further limitation of claim 2.

With regard to claims 3-5: the deeper doped region as taught by Smith is connected to zone 110 of first conductivity type (cf. column 4, lines 30-31 and column 7, lines 10-12) (*claim 3*) which is an electrode or source zone (cf. column 7, lines 8-9), while the examiner takes official notice that electrode or source zones intrinsically have a higher doping concentration than the other regions within the substrate (*claim 4*). The well-shaped region 80 extends more deeply into the substrate than said zone 110 to which it is attached (cf. Fig. 7).

1. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, and Smith as applied to claim 5 above, and further in view of Li et al (5,623,387). As detailed above, claim 5 (on which claim 6 depends) is unpatentable over Avery in view of Smith. Neither Avery, nor Smith necessarily teach the further limitation of claim 6. However, the lateral enclosure of transistors by doped zones connected through metal contacts is well known in the art as an obvious way (creation of equipotential lines

through enclosure by conductors) of creating favorable conditions for a more uniform conduction of current between emitter and collector zones in transistors, as witnessed by Li et al, who teach an esd protection circuit (cf. title) involving a bipolar transistor (cf. abstract), specifically the surrounding of first conductivity type emitter and collector zones 431, 435, by second conductivity type zones 422 connected to a common metal contact 423 (cf. Fig. 6B; see also Fig. 7B) (cf. column 13, lines 54-59). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of claim 5 so as to include the further limitation of claim 6.

2. ***Claims 7- 10 and 12*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Avery, Smith, and Li et al as applied to claim 6 above, and further in view of Wong et al (6,277,689). As detailed above, claim 6 (on which claim 7 depends) is unpatentable over Avery and Smith, in view of Li et al.

Avery, Smith, nor Li et al, necessarily teach the further limitation defined by claim 7, except for the presence of charge carriers of the first conductivity type (see Smith, column 1, lines 37-43).

However, the use of embedded wells for the purpose of combating volatility in lateral bipolar transistors is well known in the art as witnessed by Wong who teaches a P-well 34 embedded in an N-well 36 within a substrate 38 (cf. Fig. 4 and column 3, lines 60-64).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 6 at the time at the time of the invention so as to include the further limitation of claim 7.

With regard to claim 8: emitter and collector zones 42 and 44, respectively, as shown in Fig. 4 of Avery are designed as strips and are disposed in alternating fashion next to one another and parallel to one another. Thus the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: Figure 6 in Avery shows that the electrostatic discharge structure of Avery configured and arranged in an essentially square layout. Thus the further limitation of claim 9 does not distinguish over the prior art.

With regard to claim 10: the examiner takes official notice that the provision of thorough contacts between electrodes and emitter/collector regions is an obvious requirement for any transistor: without it the current through the device would be impeded and the voltage between emitter and collector would be compromised. Therefore, the further limitation of claim 10 does not distinguish over the prior art.

With regard to claim 11: The electrostatic discharge structure taught by Avery comprises emitter and collector electrodes (vertical portions of 22 and 20, respectively) connected via conductor tracks (inherent property of electrodes in any working electronics device of which they form a part) to oppositely situated voltage buses 22 and 20 (cf. Fig. 2; see col.6, l. 37-53) and form finger-like connections (four fingers on each side in Fig. 2) which are staggered with one another (staggered because marked by an alternating pattern).

With regard to claim 12: the bipolar transistor electrostatic discharge structure as taught by Avery is designed as a field oxide bipolar transistor structure, as shown by Fig. 5.

(9)-a Prior Art of Record and applied in the Final Action to appealed rejection of claim 11

5,043,782	AVERY	08-27-1991
JP 61-292351	WADA ET AL.	12-23-1986
6,147,852	RAVANELLI	11-14-2000
6,072,271	SMITH	06-13-2000
5,623,387	LI ET AL	04-22-1997
6,277,689	WONG	08-21-2001

(9)-b Other Prior Art of Record

5,449,939	Horiguchi et al.	09-12-1994
5,543,649	Kim et al.	08-06-1995
EP 0 753 892 A1	Amerasekera et al	01-15-1997
5,345,357	Pianka	09-06-1994
5,898,206	Yamamoto	04-27-1999
6,469,354	Hirata	10-22-2002

(10) Response to Argument

1. Claim 1

(A) Appellant alleges no prima facie obviousness has been presented (argument A on pages 8-9 of Appeal Brief). Examiner disagrees:

(a) *Wada et al* explicitly teach a single track resistor to precede every connection of a control most vulnerable to ESD so as to more uniformly distribute the load: see citation of the explicitly stated purpose by Wada et al to more uniformly distribute the ESD input surge voltage through polysilicon resistor 2 by Wada preceding source-drain (5/6) control in parallel transistors 4, as explained in the English Abstract and as illustrated in Figure 2. Also note that the other control (gate) has a single resistor connected to all transistors (common gate electrode 9; see page 4 of translation; second full paragraph) and hence Wada et al teach a device wherein the particular protection menas of a single track resistor distributing the load is met for all possible routes of ESD surges. It is also elementary knowledge for those of ordinary skills in the electrical art that if a load is non-uniformly distributed then the maximum load goes up, which is trivially to be avoided in art combating ESD surge damage.

(b) Ravanelli teaches as prior art in the cited portion (col. 1, l. 45+) a/o transistor in parallel with a common resistor to combat ESD (Figure 1) with motivation specifically stated.

Appellant may disagree with the statements on motivation on specifics. But is incorrect to allege no motivation has been provided.

(B) Appellant alleges no proper combination of references which discloses the invention as set forth in claim 1.

Examiner disagrees:

As the first argument in this regard Appellant alleges that in Wada et al "resistor 2 does not cause the current to be uniformly distributed" (page 10 of Appeal Brief).

However, resistor 2 is a cause thereof, as witnessed by the cited portion of the English abstract. That other means are applied as well, in particular channel length variation, but all means combined lead to the equivalent circuit of Figure 2 with single track resistor 2 every control connection.

As the second argument Appellant alleges that if the long channel lengt of the transistors QL were modified to include channel lengths of various sizes then the circuit of Avery may no longer operate for its intended purpose. However, Avery does teach both short- and long-channel transistors QL and QS respectively.

The subsequent allegation "modifying Avery according to Wada may result in an inoperable device" is not persuasive because no explanation has been provided why the device would be inoperable.

The third argument (page 11) that Ravanelli uses rather limited express language for his cited teaching is not persuasive, because the resistor integrated into the substrate of the integrated circuit so as to lead to equivalent circuit depicted in Figure 1 is evidently at the least primus inter pares among stated alternatives, as witnessed by said Figure 1. That Ravanelli "does not teach the inclusion of one track resistor as Prior Art" is not persuasive because Ravanelli clearly teaches as prior art one resistor to both gate controls of the transistors through Figure 1.The argument that "Ravanelli does not even use the singular term resistor" is not persuasive because a single resistance (prepared by including a buried doped region in the substrate, hence in essence an altered substrate rather than the p-doped substrate by Avery) is both control terminals of Q1 and Q2. Finally, on the argument that "Ravanelli does not even mention laterally

designed bipolar transistors" (page 11) at least Q1 is bipolar (see col. 3, l. 9-12) and the essential ESD protection portion is laterally designed bipolar (Figure 3), while whether or not the transistors are bipolar or MOS transistors does not necessarily enter in any of the claim limitations or obviousness arguments.

2. Claims 2-5:

Applicant's first argument is that "Smith has nothing to do with ESD protective devices" (page 12). This argument is not persuasive because Smith explicitly is about means for inhibiting ESD (see title, abstract and "Field of Invention").

Applicant's second argument is that ESD circuit 15 is not disclosed within the specification. This argument is not persuasive because ESD circuit 15 was not cited while the teaching of said deeper doped region or well-shaped region 80 is specifically cited by Smith to act as a barrier for charge carriers generated by the (ESD-produced) avalanche as explained in the office action on page 6).

3. Claim 6:

Appellant presents no arguments other than the traverse of the rejection of 5 discussed above.

4. Claims 7-12:

Appellant presents no arguments other than the traverse of the rejection of 5 discussed above.

This concludes the Response to Argument.

However, a simpler rejection could have been given, because Avery also teaches a resistor (RS) co-integrated into a semiconductor body preceding the control

connection for *all* of the aforementioned laterally designed bipolar transistors QL and QS because said resistor RS is co-integrated into the semiconductor by being constituted as the p-doped substrate (col. 4, l. 22-25 and col. 6, l. 44-46).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR

41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:

JPM
August 3, 2006
Conferees
Ricky Mack, Nathan Flynn, Johannes Mondt

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

MICRONAS GMBH
HANS-BUTNE-STRASSE 19
79108 FREIBURG
GERMANY

Approved.

JANICE A. FALCONE
DIRECTOR
TECHNOLOGY CENTER 2800

Translation of Wada et al by USPTO - Translation 5.

PTO: 2006-5779
Japanese Published Unexamined (Kokai) Patent Publication No. 61-292351; Publication Date: December 23, 1986; Application No. 60-134749; Application Date: June 20, 1985; Int. Cl.[4]: H01L 27/06 29/78; Inventor(s): Toshio Wada et al.; Applicant: Sanyo Electric Co., Ltd.; Japanese Title: Nyuryoku Hogo Kairo (Input Protection Circuit)

Specification

1. Title of Invention

Input Protection Circuit

2. Claim

An input protection circuit which is connected from an input pad to a gate electrode for a MIS transistor protected via a polysilicon resistor and a protecting MIS transistor having a predetermined source-drain breakdown voltage, characterized in that the length of a channel between a source region and a drain region of the protecting MIS transistor is reduced more than that connected to the polysilicon resistor to reduce the source-drain breakdown voltage.

3. Detailed Description of the Invention

(a) Field of Industrial Application

This invention pertains to an improved input protection circuit for a MIS transistor circuit.

(b) Prior Art

As for prior art input protection circuit, an input protection circuit that uses a diffusion resistor as shown in Fig.4 is known as disclosed in Japanese examined patent application No. 45-034641.

In Fig.4, reference number 21 refers to an input pad made from Al, and 22 to the diffusion resistor formed diffusing an impurity on a semiconductor substrate, which enters one end thereof from the input pad 21 in terms of pattern and which is connected from the other end thereof to a gate electrode of a MIS transistor protected with a wire 23 via a contact. Fig.5 is an equivalent circuit view illustrating the input protection circuit of Fig.4. The diffusion resistor 22 forms a resistor and a diode in the opposite direction between the substrate and the diffusion resistor. Input surge voltage is uniformized using a time constant circuit formed from the resistor and passes through the substrate using the diode so as to prevent breakage of a gate oxide film of the MIS transistor.

As for the other prior art input protection circuit, an input protection circuit that uses a polysilicon resistor as shown in Fig.6 is known as disclosed in Japanese unexamined patent application No. 59-74665.

In Fig.6, reference number 31 refers to an input pad made from Al, and 32 to a polysilicon resistor consisting of a N^+ polysilicon layer and being formed on an insulating film of a semiconductor substrate, which enters one end thereof from the input pad 31 via a contact in terms of pattern and which is connected from the other end thereof to a gate electrode of a MIS transistor protected with a wire 33 via a contact. Fig.7 is an equivalent circuit view illustrating the input protection circuit of Fig.6. Input surge voltage is uniformized using a time constant circuit formed from the polysilicon resistor 32 and a MOS capacity thereat so as to protect a gate oxide film of the MIS transistor.

(c) Problem to Be Solved by the Invention

At the former prior art input protection circuit, when larger input surge voltage is charged, it is added concentrating on the input pad side of the diffusion resistor 22. As a result, the PN bonding is easily broken.

At the latter prior art input protection circuit, when larger surge voltage is charged, it is also charged to the gate electrode of the MIS transistor via the polysilicon resistor 32 to break the gate oxide film because it does not have a structure to pass it through the substrate.

(d) Measures for Solving the Problem

The invention is produced in the light of the aforementioned disadvantages and so as to realize an input protection circuit with the disadvantages largely eliminated by combining the polysilicon resistor 2 and the protecting MIS transistor 4 having varied source-drain breakdown voltage by varying the channel length of the polysilicon resistor 2.

(e) Effect

According to the invention, after the uniformization of the input surge voltage using the polysilicon resistor 2, the input surge voltage is uniformly distributed to pass through an earth by varying the source-drain breakdown voltage, thereby protecting even larger surge voltage without breaking the input protection circuit.

(f) Working Example

An input protection circuit of the invention is described in detail with reference to Fig.1 to Fig.3.

Fig.1 is a top view illustrating the input protection circuit of the invention. Reference number 1 refers to an input pad made from Al; 2 to a polysilicon resistor consisting of a N^+ polysilicon layer and being formed on a field insulating film of a semiconductor substrate 3; 4 to a protecting MIS transistor characterized by the invention. At the protecting MIS transistor 4, source and drain regions 5 and 6 consisting of a N^+ diffusion layer as indicated by a dashed line are provided in a distant fashion. A step 8 is formed in a part of the drain region 6 that corresponds to a channel region 7. The step 8 is formed through an almost entire width of the channel region 7. The channel length varies from L_1 to L_2 to L_3 to L_4. More specifically, the closer the channel length L is to a gate electrode side of a MIS transistor, the shorter the length is.

In terms of pattern, the input pad 1 is connected to one end of the polysilicon resistor 2 via a contact. An Al wire builds a connection from the other end of the polysilicon resistor 2 to one end of the drain region 6 of the protecting MIS transistor 4 via a contact. A gate electrode 9 of the protecting MIS transistor 4 is connected to the source region 5 via a contact while it is covered with a gate oxide film on the channel region 7 and further connected to an earth or a power source. A gate electrode 10 of the MIS transistor to be protected is connected to the other end of the drain region 6.

Fig.2 is an equivalent circuit view of Fig.1 by the invention. The input pad 1 and the gate electrode of the MIS transistor to be protected are connected via multiple protecting MIS transistors 4 with various source-drain breakdown voltages by varying the polysilicon resistor 2 and the channel length L. At the multiple protecting MIS transistors,

the channel length L is gradually reduced from a polysilicon resistor side. A source-drain breakdown voltage V_T is also predetermined so as to be gradually reduced. Input surge voltage is uniformly dispersed in each protecting MIS transistor.

The operation of the input protection circuit of the invention is described. As described above, the protecting MIS transistor is designed so that the channel length L is gradually reduced to L_1 to L_2 to L_3 to L_4. If the channel length is gradually reduced to L_1=7 μm to L_2=3 μm to L_3=2 μm to L_4=1.5 μ, a source-drain breakdown voltage BV_{DS} varies from 21V to 17V to 14V to 12V as shown in Fig.3. In Fig.3, a protecting MIS transistor having a concentration of an impurity on the surface of a field of a P type silicon substrate of 10 Ωcm at 2 x 10^{16} cm^{-3}, a gate oxide film thickness t_{ex} at 400Å and a diffusion depth xj of source and drain regions at 0.5 μm is used as an example. On the other hand, the protecting MIS transistor is designed defining the protection gate withstand pressure at about 15V. At an input protection circuit of the protecting MIS transistor, larger input surge voltage can pass through an earth on a side where the transistor is connected to the polysilicon resistor 2 having larger source-drain breakdown voltage BV_{DS}. Smaller input surge voltage can pass through an earth on a gate electrode side that has smaller source-drain breakdown voltage BV_{DS}. Thereby, the input surge voltage can be uniformly dispersed in the protecting MIS transistor according to the intensity of the source-drain breakdown voltage BV_{DS}. Accordingly, the source-drain breakdown voltage BV_{DS} can be predetermined larger than the about 15V protection gate withstand pressure of the MIS transistor to be protected on the polysilicon resistor side and smaller than the protection gate withstand pressure on the gate electrode side. In order to prevent the breakage of a PN bonding at the drain region 6 of the protecting MIS

transistor, the source-drain breakdown voltage BV_{DS} thereof needs to be designed smaller than about 30V of the PN bonding withstand pressure.

At the aforementioned working example, a protecting MIS transistor with an Al gate structure is used. A protecting MIS transistor with a Si gate structure can also be used to achieve the purpose of the invention.

(g) Advantageous Effect of the Invention

According to the invention, because the source-drain breakdown voltage BV_{DS} is gradually reduced by gradually reducing the channel length L of the protecting MIS transistor, the input surge voltage is uniformly dispersed in the channel thereof. Thus, the gate oxide film of the MIS transistor can be stably protected regardless of the intensity of the input surge voltage if it is smaller or larger.

Because the polysilicon resistor 2 is used at the invention, the same resistance value is realized at an area smaller than that of the diffusion resistor, thereby contributing to minimization of the input protection circuit.

Furthermore, because the input surge voltage is dispersed to pass through the earth using the protecting MIS transistor at the invention, the protecting MIS transistor rarely brakes due to larger input surge voltage, thereby attaining an input protection circuit highly resistant to breakdown strength.

4. Brief Description of the Drawings

Fig.1 is a top view illustrating an input protection circuit of the invention. Fig.2 is an equivalent circuit view illustrating the input protection circuit of the invention. Fig.3 is

a characteristic view illustrating an operation of the invention. Fig.4 and Fig.6 are top views illustrating prior art input protection circuits. Fig.5 and Fig.7 are equivalent circuit views illustrating prior art input protection circuits of Fig.4 and Fig.6.

Description of the Main Reference Numbers

1...Input pad

2...Polysilicon resistor

4...Protecting MIS transistor

5 and 6...Source-drain regions

7...Channel region

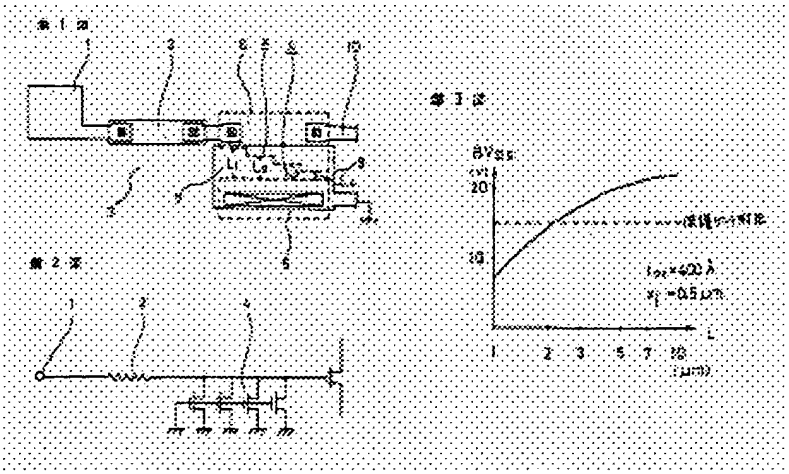

Fig.3:
Dashed line: Protection gate withstand pressure

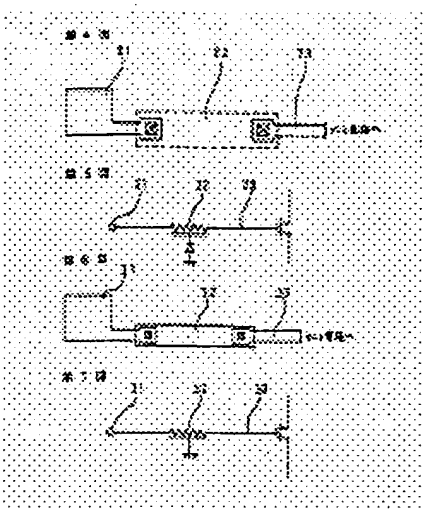

Fig.4:
To the gate electrode

Fig.6:
To the gate electrode

U.S. Patent and Trademark Office
Translations Branch
7/13/06
Chisato Morohashi